Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

Claims 1 - 5 (cancelled)

6. (currently amended) ~~The system recited in claim 5~~ A data storage system wherein a host computer is coupled to a bank of disk drives through an interface, such interface comprising:

a plurality of directors;

a bus;

a memory connected to the directors through the bus;

wherein the directors control data transfer between the host computer and the bank of disk drives as such data passes through the memory;

a plurality of ESCON adapters, a front end portion of the directors being coupled between the host computer and the bus through the ESCON adapter boards;

wherein each one of such adapter boards includes:

a plurality of adapter board ports each one being coupled to a corresponding port of the host computer;

a plurality of adapter board gate arrays;

a plurality of optic interfaces, each one of the optic interfaces being coupled between a corresponding one of the adapter board ports and a corresponding one of the adapter board gate arrays, each one of the coupled optic interfaces and adapted board gate arrays providing a corresponding one of a plurality of channels for the data;

wherein each adapter board also comprises:

a plurality of adapter board CPUs, each one being coupled to the adapter board gate arrays and the optic interface of a corresponding one of the channels, each one of the CPUs controlling the initiation and termination of the data passing through said corresponding one of the channels;

wherein each one of the front end portion of the director boards includes a plurality of director board gate arrays and a plurality of EDACs; and

wherein each pair of the director board gate arrays is coupled between a corresponding pair of the adapter board gate arrays and a corresponding one of the EDACs.

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7. (original) The system recited in claim 6 including a plurality of director board CPUs each one is coupled to a corresponding one of the adapter board CPUs, each one of the director board CPUs being coupled to a corresponding one of the director board gate arrays to control the initiation and termination of a data transfer through such coupled one of the director gate arrays.

8. (currently amended) The system recited in claim 7 including a common state machine coupled to the plurality of director gate arrays and the plurality of EDACs for arbitrating between the pair of director board gate arrays coupled to the corresponding one of the EDACs for access to such corresponding one of the EDACs.

9. (currently amended) The system recited in claim 8 wherein each one of the directors comprises: a plurality of dual port RAMs, each one being coupled to a corresponding one of the EDACs and to the bus; ~~at least one of the busses;~~ and, a second common state machine coupled to the first common state machine and the

plurality of dual port RAMs for arbitrating between the plurality of dual port RAMS for access to ~~one the at least one of~~ the bus~~busses~~.